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10/719,814	11/21/2003	Naoyuki Kamei	60341 (70904)	3310

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,814	KAMEI ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-17,19 and 20* is/are rejected.

7)☐ Claim(s) *8 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20, as amended on 9/8/2006, are pending in the instant application. Applicant's arguments submitted 9/8/2006 have been carefully and fully considered, but they are not persuasive. Accordingly, this Office action is made **FINAL**.

Claim Rejections - 35 USC § 112

2. The rejection of claims 6 and 16 under 35 USC 112 second paragraph has been withdrawn.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-3, 5-7, 9-13, 15-17, and 19-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al. (US 6,332,196).

4. **Claim 1** is taught by Kawasaki as:

a. *A CPU, comprising: a cache.* Hard disk controller (HDC) 21 of figure 4 contains buffer memory 211, which caches data read from and written to the disks 11.

b. *Power supplying means for supplying power to an external memory, wherein the CPU controls the power supplying means so that power supply to the external memory is stopped when access to the external memory is inhibited.* Power control section 215 is shown in column 12 lines 57-61 to control supplying

power to the R/W circuit 18 and the disk control section 214. Column 13 lines 28-40 show that when the buffer memory is filled, the power supply to the hardware components relating to the disk access is stopped. Column 13 lines 42 48 show that if the sector requested by a read command is held in the buffer memory, it is returned to the host without restarting the power supply to the R/W related circuits.

c. *Control means.* Buffer control section 213 of figure 4.

d. *Wherein data are written into the cache and write back is performed to reflect the data written into the cache to an external memory at a desired timing.* Column 14 lines 57-64 shows that when data is written, it is stored into the buffer memory 211 to be written to disk when the buffer control section sends an interrupt to the CPU 20. Column 16 lines 48-52 show that the data to be written is written to the disk 11.

e. *The control means determining whether or not processing of a task is possible only with access to the cache in accordance.with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory.* Column 13 lines 42-46 shows that the buffer control section returns the data from the buffer memory if it is stored in the buffer memory.

5. **Claim 2** is taught by Kawasaki as:

f. The CPU according to claim 1, wherein: the control means detect free space in the cache and/or the amount of memory needed to process a task. Column 13 lines 28-31 show that a preread operation is continued until the buffer memory is filled, which shows detecting free space in the cache.

6. **Claim 3** is taught by Kawasaki as:

g. The CPU according to claim 2, wherein: in a situation where access to the external memory is inhibited, when the control means determine that the processing is impossible only with access to the cache, or when a cache miss occurs, the control means permit access to the external memory. Column 12 lines 65-66 show that in a read, data from the disk is transferred to the buffer memory. Column 13 lines 42-48 show that data is read from the buffer if there is a cache hit. If there is a cache miss, the disk must be accessed to provide the requested data.

7. **Claim 5** is taught by Kawasaki as:

h. The CPU according to claim 1, wherein: the control means detect an address of a location where unnecessary data are stored in the cache and then free a cache space corresponding to the detected address. Column 17 lines 18-23 show disk pointer 213b, which stores an address for the buffer memory where data read from the disk is to be stored. The space corresponding to the disk

pointer is a cache space that is freed because the data in the cache buffer at that location has already been transferred.

8. **Claim 6** is taught by Kawasaki as:

i. The CPU according to claim 1, wherein: at the start-up of the CPU, access to the external memory is inhibited after a program and data are loaded into the cache from the external memory. Column 18 lines 15-19 show that when the buffer memory is full, the preread is stopped and the power supply to the hardware relating to the disk access is stopped. It is inherent that this occurs after the HDC has been powered on, and the HDC must receive power to operate. As is known by one of ordinary skill in the art, programs and data are stored on and read from disks.

9. **Claim 7** is taught by Kawasaki as:

j. The CPU according to claim 1, wherein: the control means determine whether or not access to the external memory is needed when a state of a task changes. Column 18 lines 7-19 shows that the buffer control section detects when the host pointer and the disk pointer are equal, which indicates that the buffer is in a full state. When the buffer control section detects this, it stops the preread and instructs the CPU to stop the power supply to the disk access hardware.

10. **Claim 9** is taught by Kawasaki as:

k. *An information processing device comprising: a CPU which writes data into a cache provided therein and performs write back to reflect the written data into the cache to an external memory at a desired timing the external memory.* Column 14 lines 57-64 shows that when data is written, it is stored into the buffer memory 211 to be written to disk when the buffer control section sends an interrupt to the CPU 20. Column 16 lines 48-52 show that the data to be written is written to the disk 11.

l. *And power supplying means for supplying power to the external memory.* Power control section 215 of figure 4.

m. *The CPU including control means for determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory.* Column 13 lines 42-46 shows that the buffer control section returns the data from the buffer memory if it is stored in the buffer memory.

n. *The power supplying means stopping power supply to the external memory when access to the external memory is inhibited.* Power control section 215 is shown in column 12 lines 57-61 to control supplying power to the R/W circuit 18 and the disk control section 214. Column 13 lines 28-40 show that when the buffer memory is filled, the power supply to the hardware components relating to the disk access is stopped. Column 13 lines 42 48 show that if the

sector requested by a read command is held in the buffer memory, it is returned to the host without restarting the power supply to the R/W related circuits.

11. **Claim 10** is taught by Kawasaki as:

o. The information processing device according to claim 9, the external memory includes a plurality of modules. See R/W circuit 18 and disk control section 214 of figure 4.

p. And the control means control power supply with respect to each of the modules. Column 12 lines 46-52 show that power supply is stopped to the disk control section and the R/W circuit.

12. **Claim 11** is taught by Kawasaki as:

q. A controlling method of a CPU which writes data into a cache included therein and performs write back to reflect the data written into the cache to an external memory at a desired timing. Column 14 lines 57-64 shows that when data is written, it is stored into the buffer memory 211 to be written to disk when the buffer control section sends an interrupt to the CPU 20. Column 16 lines 48-52 show that the data to be written is written to the disk 11.

r. The method comprising the steps of: determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and when it is determined that the processing is possible, inhibiting access to the external memory.

Column 13 lines 42-46 shows that the buffer control section returns the data from the buffer memory if it is stored in the buffer memory. By determining that the requested data is held in the buffer memory, the HDC is determining if it is possible to process a task, returning requested data to the host, by only accessing the cache, buffer memory 211.

s. Wherein when access to the external memory is inhibited, power supply to the external memory is stopped. Power control section 215 is shown in column 12 lines 57-61 to control supplying power to the R/W circuit 18 and the disk control section 214. Column 13 lines 28-40 show that when the buffer memory is filled, the power supply to the hardware components relating to the disk access is stopped. Column 13 lines 42 48 show that if the sector requested by a read command is held in the buffer memory, it is returned to the host without restarting the power supply to the R/W related circuits.

13. **Claim 12** is taught by Kawasaki as:

t. The method according to claim 11, further comprising the step of: detecting free space in the cache and/or the amount of memory needed to process a task. Column 13 lines 28-31 show that a preread operation is continued until the buffer memory is filled, which shows detecting free space in the cache.

14. **Claim 13** is taught by Kawasaki as:

u. The method according to claim 12, further comprising the step of: in a situation where access to the external memory is inhibited, when it is determined that the processing is impossible only with access to the cache, or when a cache miss occurs, permitting access to the external memory. Column 12 lines 65-66 show that in a read, data from the disk is transferred to the buffer memory. Column 13 lines 42-48 show that data is read from the buffer if there is a cache hit. If there is a cache miss, the disk must be accessed to provide the requested data.

15. **Claim 15** is taught by Kawasaki as:

v. The method according to claim 11, further comprising the steps of: detecting an address of a location where unnecessary data are stored in the cache; and freeing a cache space corresponding to the detected address. Column 17 lines 18-23 show disk pointer 213b, which stores an address for the buffer memory where data read from the disk is to be stored. The space corresponding to the disk pointer is a cache space that is freed because the data in the cache buffer at that location has already been transferred.

16. **Claim 16** is taught by Kawasaki as:

w. The method according to claim 11, further comprising the step of: at the start-up of the CPU, inhibiting access to the external memory after a program and data are loaded into the cache from the external memory. Column 18 lines

15-19 show that when the buffer memory is full, the preread is stopped and the power supply to the hardware relating to the disk access is stopped. It is inherent that this occurs after the HDC has been powered on, and the HDC must receive power to operate. As is known by one of ordinary skill in the art, programs and data are stored on and read from disks.

17. **Claim 17** is taught by Kawasaki as:

x. The method according to claim 11, further comprising the step of: determining whether or not access to the external memory is needed when a state of a task changes. Column 18 lines 7-19 shows that the buffer control section detects when the host pointer and the disk pointer are equal, which indicates that the buffer is in a full state. When the buffer control section detects this, it stops the preread and instructs the CPU to stop the power supply to the disk access hardware.

18. **Claim 18**

y. The method according to claim 11, further comprising the steps of: determining whether or not a program and data in the cache are purged; and if not purged, avoiding loading the program and the data into the cache from the external memory.

19. **Claim 19** is taught by Kawasaki as:

z. *A CPU comprising a cache*. Hard disk controller (HDC) 21 of figure 4 contains buffer memory 211, which caches data read from and written to the disks 11.

aa. *Power supply which supplies power to an external memory, wherein the CPU controls the power supply so that power supply to the external memory is stopped when access to the external memory is inhibited.* Power control section 215 is shown in column 12 lines 57-61 to control supplying power to the R/W circuit 18 and the disk control section 214. Column 13 lines 28-40 show that when the buffer memory is filled, the power supply to the hardware components relating to the disk access is stopped. Column 13 lines 42 48 show that if the sector requested by a read command is held in the buffer memory, it is returned to the host without restarting the power supply to the R/W related circuits.

bb. *And controller*. Buffer control section 213 of figure 4.

cc. *Wherein data are written into the cache and write back is performed to reflect the data written into the cache to the external memory at a desired timing.* Column 14 lines 57-64 shows that when data is written, it is stored into the buffer memory 211 to be written to disk when the buffer control section sends an interrupt to the CPU 20. Column 16 lines 48-52 show that the data to be written is written to the disk 11.

dd. *The controller determines whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is*

possible, inhibiting access to the external memory. Column 13 lines 42-46 shows that the buffer control section returns the data from the buffer memory if it is stored in the buffer memory.

20. **Claim 20** is taught by Kawasaki as:

ee. An information processing device comprising a CPU which writes data into a cache provided therein and performs write back to reflect the written data into the cache to an external memory at a desired timing. Column 14 lines 57-64 shows that when data is written, it is stored into the buffer memory 211 to be written to disk when the buffer control section sends an interrupt to the CPU 20. Column 16 lines 48-52 show that the data to be written is written to the disk 11.

ff. The external memory. Disks 11 of figure 4.

gg. And power supply which supplies power to the external memory. Power control section 215 is shown in column 12 lines 57-61 to control supplying power to the R/W circuit 18 and the disk control section 214.

hh. Wherein the CPU including a controller which determines whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory. Column 13 lines 42-46 shows that the buffer control section returns the data from the buffer memory if it is stored in the buffer memory.

ii. And wherein the power supply stops power supply to the external memory when access to the external memory is inhibited. Column 13 lines 28-40 show that when the buffer memory is filled, the power supply to the hardware components relating to the disk access is stopped. Column 13 lines 42 48 show that if the sector requested by a read command is held in the buffer memory, it is returned to the host without restarting the power supply to the R/W related circuits.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (cites *supra*) in view of Ramsey et al. (US 5,813,022).

23. **Claim 4** is taught by Kawasaki as shown *supra* with respect to claim 1

24. Kawasaki does not disclose expressly controlling a clock frequency of an internal clock.

25. With respect to claim 4, Ramsey teaches:

jj. *The CPU according to claim 1, further comprising: clock control means for controlling a clock frequency of an internal clock.* Column 2 lines 23-33 of Ramsey teaches entering a stop grant state when a signal to slow or stop the computer system clock signal is asserted. Column 9 lines 3-5 of Ramsey shows that when the microprocessor is in a stop grant state the clock input can be changed.

kk. *The clock control means changing the clock frequency when access to the external memory is inhibited.* Column 13 lines 28-40 of Kawasaki show that when the HDC stops the preread, the CPU stops the power supply to the R/W related circuits and is set in a standby state.

26. Kawasaki and Ramsey are analogous art because they are from a similar problem solving area, power saving in computer systems.

27. At the time of the invention it would have been obvious to one of ordinary skill in the art to change the clock frequency of the CPU of Kawasaki as taught by Ramsey.

28. The motivation for doing so would have been to conserve energy, Ramsey column 2 lines 35-37, which is also a goal of Kawasaki, Kawasaki column 3 lines 15-21.

29. Therefore it would have been obvious to combine Ramsey with Kawasaki for the benefit of improved power savings to obtain the invention as specified in claim 4.

30. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (cites *supra*) in view of Ramsey et al. (US 5,813,022).

31. **Claim 14** is taught by Kawasaki as shown *supra* with respect to claim 11

32. Kawasaki does not disclose expressly controlling a clock frequency of an internal clock.

33. With respect to claim 14, Ramsey teaches:

II. *The method according to claim 11, further comprising the step of: when access to the external memory is inhibited, changing a clock frequency of an internal clock.* Column 2 lines 23-33 of Ramsey teaches entering a stop grant state when a signal to slow or stop the computer system clock signal is asserted. Column 9 lines 3-5 of Ramsey shows that when the microprocessor is in a stop grant state the clock input can be changed. Column 13 lines 28-40 of Kawasaki show that when the HDC stops the preread, the CPU stops the power supply to the R/W related circuits and is set in a standby state.

34. Kawasaki and Ramsey are analogous art because they are from a similar problem solving area, power saving in computer systems.

35. At the time of the invention it would have been obvious to one of ordinary skill in the art to change the clock frequency of the CPU of Kawasaki as taught by Ramsey.

36. The motivation for doing so would have been to conserve energy, Ramsey column 2 lines 35-37, which is also a goal of Kawasaki, Kawasaki column 3 lines 15-21. Therefore it would have been obvious to combine Ramsey with Kawasaki for the benefit of improved power savings to obtain the invention as specified in claim 14.

Response to Arguments

37. Applicant's arguments filed 9/8/2006 have been fully considered but they are not persuasive.

38. **First point of Argument**

39. At lines 8-10 of page 12 of the arguments submitted 9/8/2006, Applicant argues that Kawasaki does not disclose "*inhibiting access to an external memory when the processing of a task is possible only with access to a cache (and not with any access to the external memory)*". The Examiner respectfully disagrees. As noted in column 13 lines 41-48 of Kawasaki, if a read command issued by the host can be fulfilled by the data stored in buffer memory 211, the HDC 21 transfers the data already stored in buffer memory 211 through buffer control section 213 and host I/F control section 212 without intervention of the CPU 20. As shown in column 11 lines 31-40, CPU 20 is responsible for controlling the HDD. By explicitly stating that the data is transferred to the host without the intervention of the CPU, Kawasaki teaches that access to the external memory (the HDD, which is external to HDC 21) is inhibited when the processing of a task (the read request received from the host) is possible only with access to a cache (the buffer memory 211). The Examiner respectfully notes that independent claims 1, 9, 11, 19 and 20 do not require that access to an external memory is inhibited when it is determined that a task can be completely processed only with access to the cache, or that the determination as to whether or not a task can be processed only with access to the cache be determined prior to execution of the task.

40. **Second point of Argument**

41. At lines 10-12 of page 12 of the arguments filed 9/8/2006, Applicant argues that Kawasaki does not disclose "*stopping the supply of power to the external memory when access to the external memory is inhibited*". The Examiner respectfully disagrees. Column 13 lines 28-40 discuss that during a preread operation, buffer memory 211 is filled with the preread data. When the buffer memory becomes full and the preread by the HDC is stopped, CPU 20 stops power supply by the power control section to the hardware components (R/W related circuits) and is set in a standby state. Column 13 continues in lines 41-48 to discuss the HDC satisfying a read request from the host with data stored in the buffer memory with intervention of the CPU. At column 13 lines 48-63, Kawasaki discloses that when space is detected in buffer memory 211, an interrupt signal is delivered to CPU 20. This interrupt signal is delivered when there is empty space in the buffer memory, and therefore occurs after the read request has been processed. Column 13 line 64 to column 14 line 4 states that when the CPU 20 receives the interrupt signal, "*the CPU 20 controls the power control section 215 and resumes power supply to the hardware components relating to the disk access, power to which has been halted, that is, to the R/W circuit 18 and the disk control section 214 within the HDC 21, other than the registers which have already been powered (step A4).*" (emphasis added).

Allowable Subject Matter

42. **Claims 8 and 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

43. **Claim 8** recites the limitation "*wherein: the control means determine whether or not a program and data in the cache are purged, and then, if not purged, avoid loading the program and the data into the cache from the external memory*". This limitation is not taught or suggested by Kawasaki taken alone or combined with the other prior art of record.

44. **Claim 18** recites the limitation "*further comprising the steps of: determining whether or not a program and data in the cache are purged; and if not purged, avoiding loading the program and the data into the cache from the external memory.*" This limitation is not taught or suggested by Kawasaki taken alone or combined with the other prior art of record.

Conclusion

45. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
Art Unit 2187

jir

Brian R. Peugh
Primary Examiner
11/6/06